IN THE SPECIFICATION

Please amend the specification as follows.

Please replace the paragraph that begins on page 1, line 17 with the following:

This application claims priority under 35 USC §119 to provisional application no. 60/269,225 entitled "Method and Apparatus for Providing a Gigabit Ethernet Circuit Pack" filed on February 14, 2001, and to provisional patent application 60/289,940 entitled "System and Method for Recovering RZ Formatted Data Using NRZ Clock and Data Recovery," having inventors Nicholas J. Possley and David B. Upham, filed May 9, 2001, the disclosures of each of is incorporated herein by reference for all purposes.

Please replace the paragraph that begins on page 9, line 18 with the following:

Moreover, in addition to inverse multiplexing the 9-bit data into eight STS-3 signals, the inverse multiplexer 130 is further configured to provide variable byte stuffing. Then, the eight STS-3 signals, each at a data rate of 155.52 Mbits/second + offset Δ with all eight STS-3 signals synchronized and frame aligned, are provided to a modem 140 for transmission via the optical transmission line to the drop side. In particular, the modem 140 includes eight modulators one for each STS-3 signal output from the STS-3 inverse multiplexer 130. More specifically, each of the eight modulators together comprising the modem 140 is similar to modulator as described in pending U.S. Patent Application No. 09/571,349, filed May 16, 2000, now abandoned, by inventors David A. Pechner and Laurence J. Newell entitled "Through-Timing of Data Transmitted Across an Optical Communications System Utilizing Frequency Division Multiplexing" assigned to the assignor of the present application, and the disclosure of which is incorporated herein by reference for all purposes.

Please replace the paragraph that begins on page 14, line 8 with the following:

Figure 7 is a tabular illustration of a pseudo STS-3 frame for use in multiplexing VRH-RZ (Variable Rate High Speed-RZ) data. Referring to Figure 7, for the 1,129.984 Mb/s RZ signal, the data is multiplexed into the pseudo STS-3 frame for VRH-RZ data

table 700 shown in Figure 7 in blocks of 10-bits at 112.9984 MHz. For the 564.992 Mb/s signal, the data is multiplexed into the pseudo STS-3 frame for VRH-RZ data table 700 shown in Figure 7 in blocks of 5-bits at 112.9984 MHz. This allows the same clock and logic structure to be reused. Again, the byte definition of each of the entries in the pseudo STS-3 frame for VRH-RZ data table 700 of Figure 7 can be found in Figure 8. A skilled artisan would have available a variety of methods to interface to RZ signals, several approaches of which are disclosed in ~~pending~~ provisional application No. 60/289,940 entitled, "System and Method for Recovering RZ Formatted Data Using NRZ Clock and Data Recovery," having inventors Nicholas J. Possley and David B. Upham, filed on May 9, 2001.

Please replace the paragraph that begins on page 16, line 24 with the following:

As discussed above, in accordance with one embodiment of the present invention, in the add direction, the Gigabit Ethernet, RZ signals, or Fiber Channel data is inverse multiplexed into eight pseudo STS-3 data streams. The data network system 100 then modulates and sums the data stream with all other data streams for transport over an optical fiber connection. At the far end, the data network system 100 receives the eight pseudo STS-3 signals from the modem 140 and multiplexes the data back into the original high speed data stream. ~~Pending~~ U.S. Patent Application No. 09/851,593, now abandoned, entitled "Variable Rate High-Speed Input and Output in Optical Communication Network," having inventors Tian Shen, Robert B. Clarke, Jr., Thomas J. Roman, David B. Upham, David A. Pechner, and Laurence J. Newell, filed May 8, 2001, and assigned to the assignee of the present application, ~~Kestrel Solutions, Inc.,~~ provides additional examples of variable rate high speed input and output in an optical network using optical frequency division multiplexing, the disclosure of which is incorporated in its entirety by reference for all purposes.

Please replace the paragraph that begins on page 17, line 20 with the following:

In one aspect of the present invention, a Gigabit Ethernet Circuit Pack proposed by the assignee of the present invention~~, Kestrel Solutions,~~ is configured to provide an

additional interface added to the low speed shelf, the added interfaces including 1250 Mbps Gigabit Ethernet, 1062.5 Mbps Fiber Channel, 1129.984 Mb/s Return-to-Zero (RZ) data and 564.992 Mbps RZ data. The circuit pack is thus configured to provide the functionality of transparently transporting these signal formats through the backend of a data network which is through-timed from the input signals

Please replace the two paragraphs that begin on page 11, line 21 with the following:

"Figure 3 illustrates an overall system configured for transporting OC-48 optical signals in the add direction in accordance with one embodiment of the present invention. Referring to Figure 3, there is provided a pair of Clock and Data Recovery (CDRs) 310 each configured to receive Gigabit Ethernet data. Also shown in Figure 3 are Deserializers (DES) 320 configured to receive the data and the clock signal from the corresponding CDR 310 and output a parallel 10-bit data each. The clock signal from the CDR 310 is also provided to the divider 330 which is configured to divide the clock signal from the CDR 310 by a factor of 10. The parallel 10-bit data from the DES 320 is provided to the 10-bit to 9-bit translation unit 340 which is configured to translate the parallel 10-bit data received from the DES 320 into respective corresponding parallel 9-bit data. The parallel 9-bit data from each 10-bit to 9-bit translation unit 340 is then provided to the elastic store unit 350. The elastic store unit 350 in one embodiment is configured to perform buffering of the data during the time the multiplexer is transmitting frame overhead or bit stuffing.

As further shown in Figure 3, the clock signal divided by the divider 330 is provided to the 10-bit to 9-bit translation unit 340 as well as to the elastic store unit 350. The parallel 9-bit data from ~~the~~ each elastic store unit 350 is provided to STS-48c Mapper/Scrambler 360 which is also configured to receive a clock signal from the multiplexer clock 370. As further shown, the multiplexer clock is also provided to each elastic store units 350. Additionally, the STS-48c Mapper/Scrambler 360 is also configured to receive overhead data from the STS-48c overhead generator 380 as well as

a 155.52 MHz clock signal. The 16-bit STS-48c data output from the STS-48c Mapper/Scrambler 360 is then provided to serializer/optical transceiver 390 which is then configured to transmit OC-48c data to the remote side."